

FIG. 1

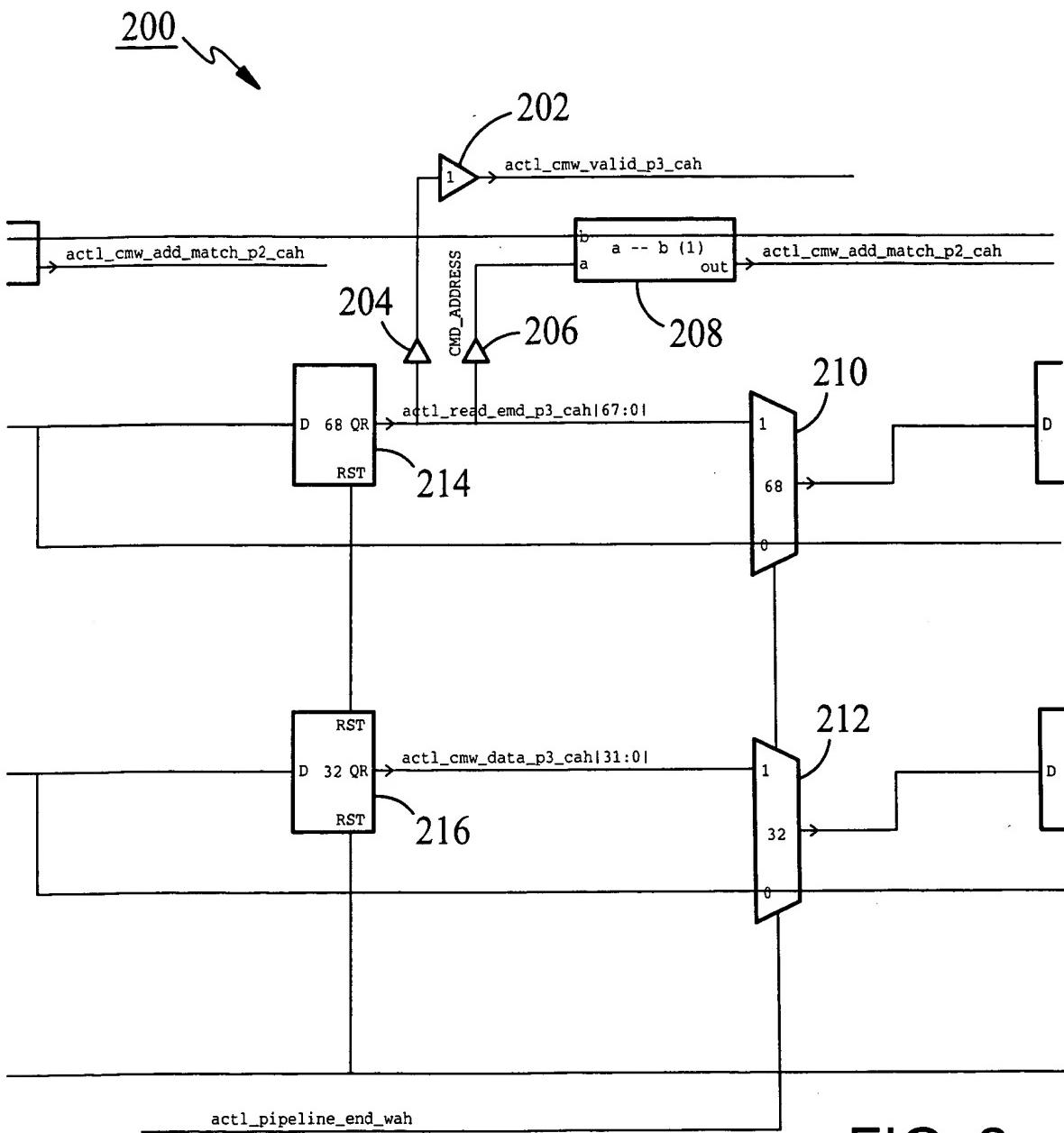


FIG. 2

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 Applicant(s): William R. Wheeler et al.
 LOGIC SIMULATION

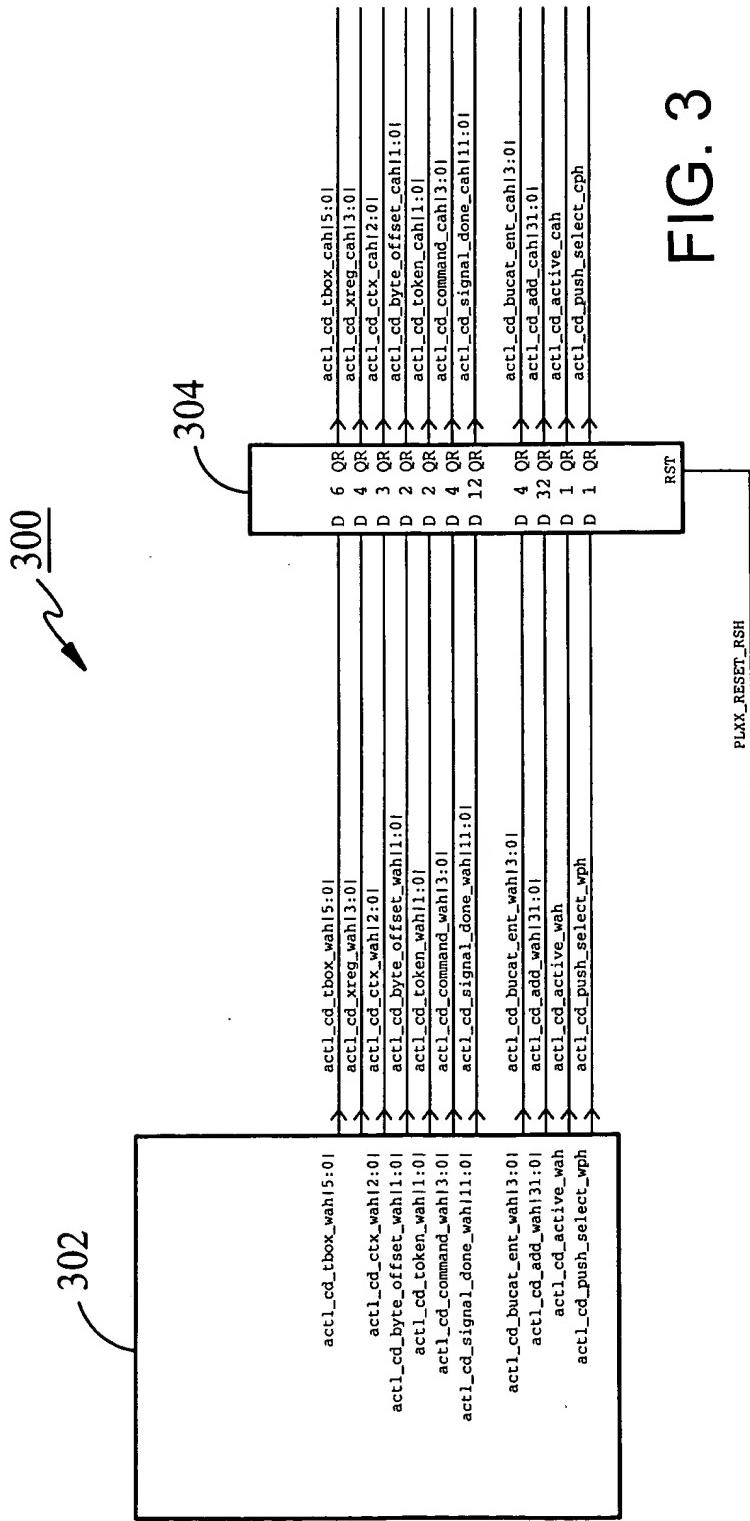


FIG. 3

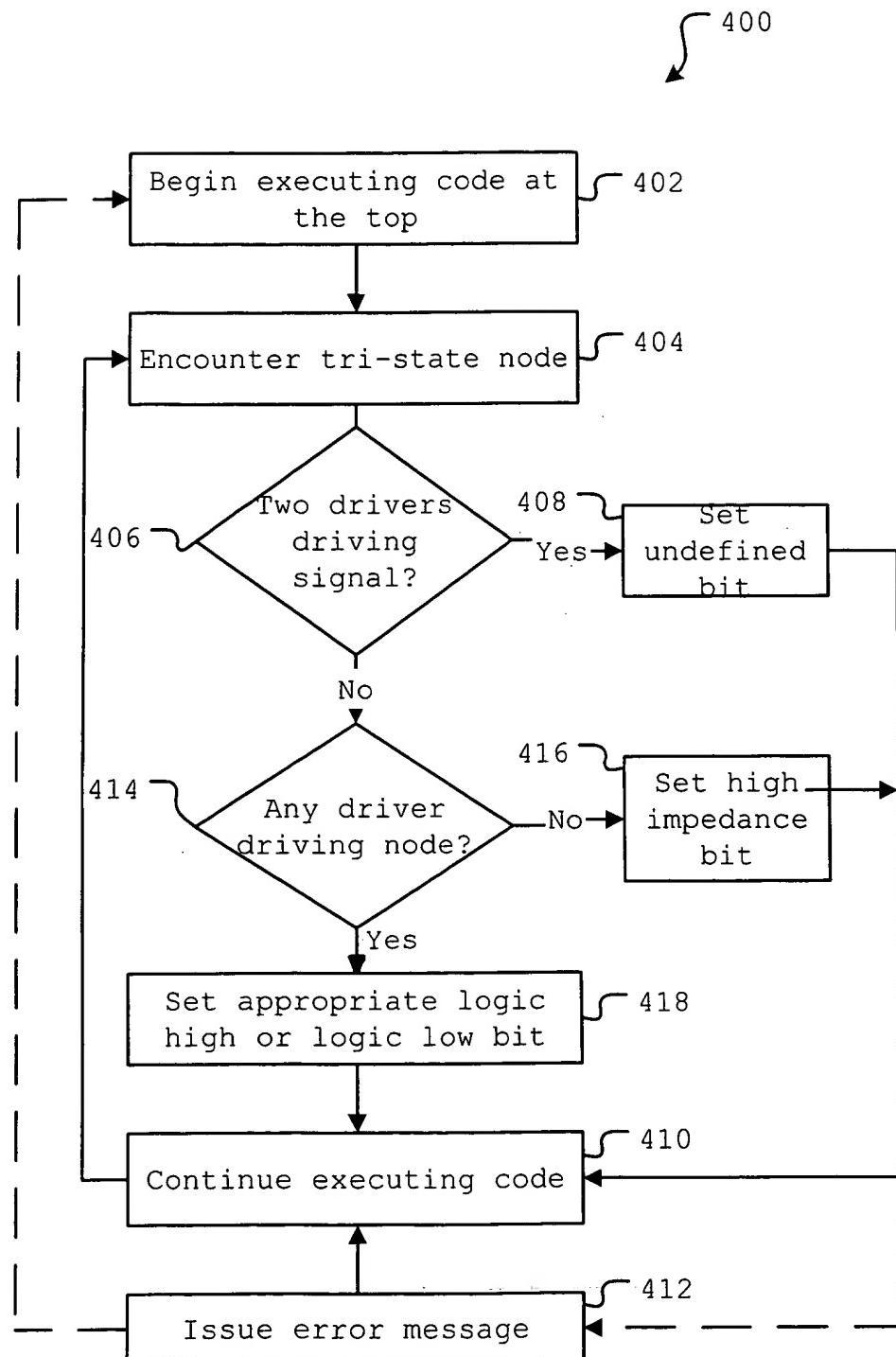


FIG. 4

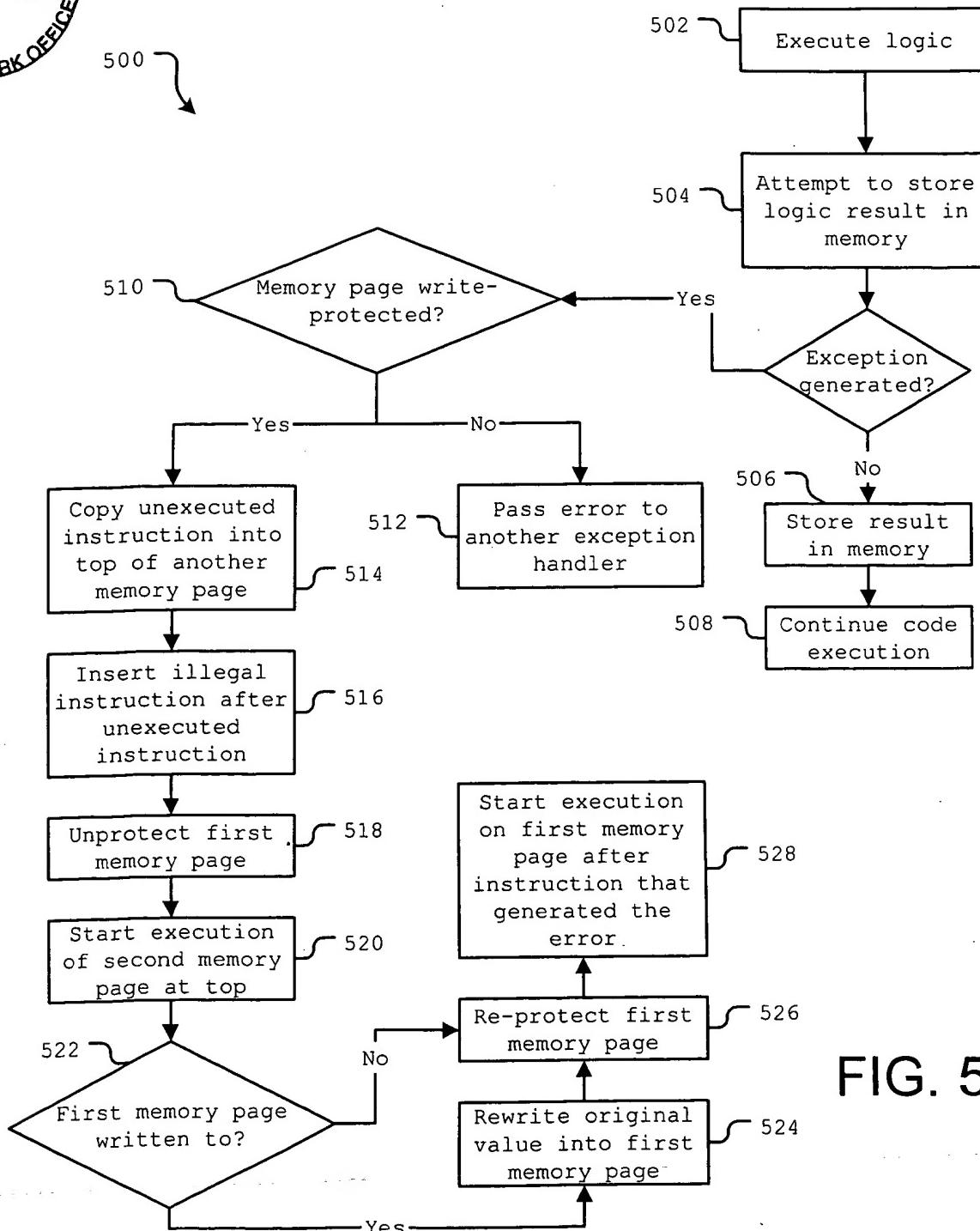


FIG. 5

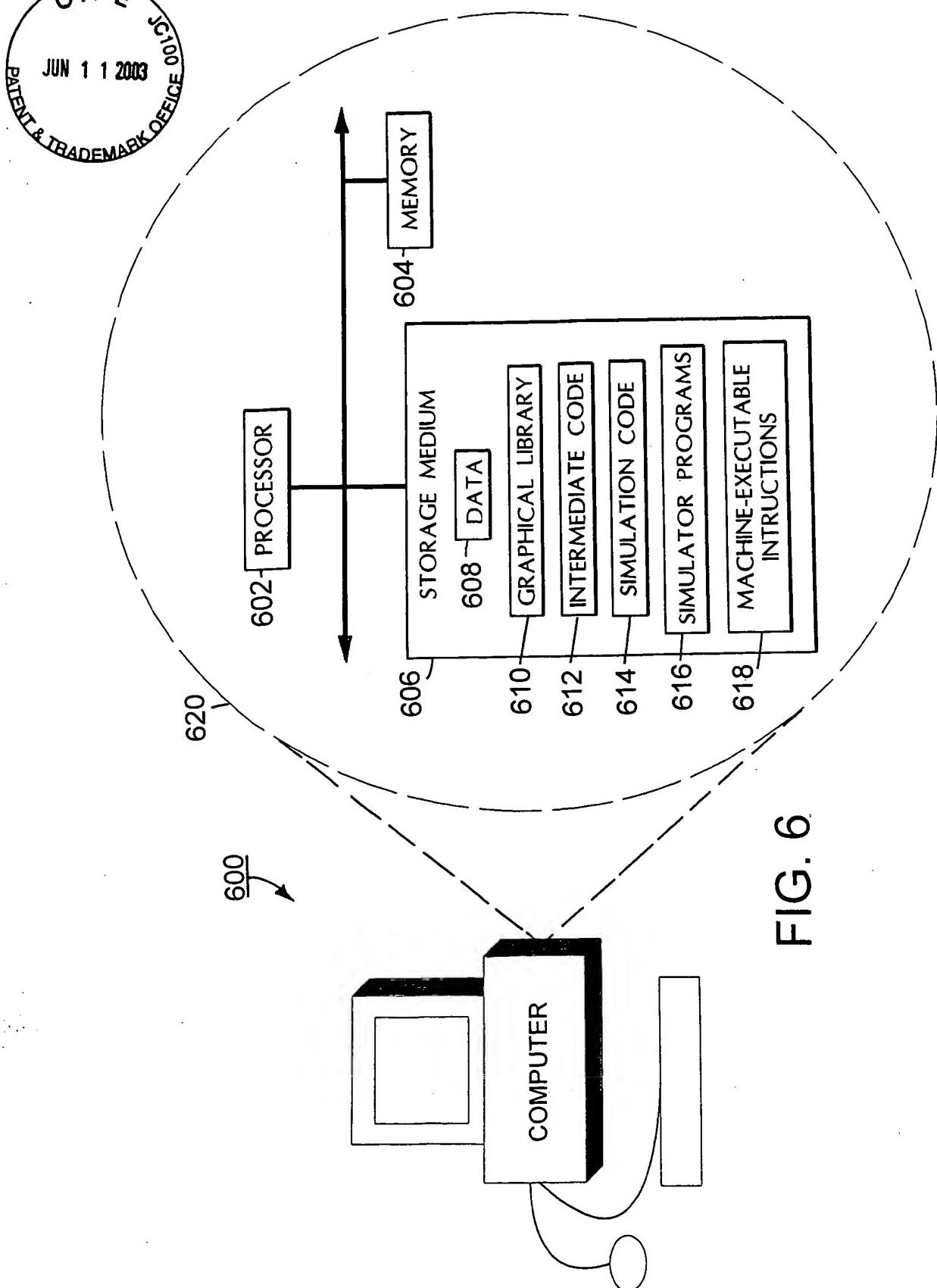


FIG. 6